PCIB40

40-Ch Digital I/O & Counter Board

Technical Manual

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Arcom CONTROL SYSTEMS

Preface

Packing List

This product is shipped as follows:

- Board
- User Manual
- Utility Disk
- PCbus Library Datasheet

If any of the above appear to be missing, please telephone Arcom 01223 411200.

Utility Disk

This product is shipped with a utility disk which contains:

- PCbus library Manual
- Source Code for all PCbus I/O boards
- A test program called TEXT.EXE

Handling

This board contains CMOS devices which could be damaged in the event of static electricity being discharged through them. At all times please observe anti-static precautions when handling the board and always unpack and install the board in an anti-static working area.

Please ensure that should a board need to be returned to Arcom, it is adequately packed and if a battery is fitted, that it is isolated.

Product Information

Full information about other Arcom Products is available via the **Fax on Demand System**, (Telephone Numbers are listed below), or by contacting our **WebSite** in the UK at: **www.arcom.co.uk**, or in the US at: **www.arcomcontrols.com**

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Revision History

Manual	PCB	Comments	
Issue A	V3 I3	960514	
Issue B	V3 I4	970520	[ECO2486]
Issue C	V3 I4	980119	[ECO2684]

Introduction

The PCIB40 is an 8-bit ISA bus add-on board providing 40 channels of digital I/O and three 16-bit counter/timers. The digital I/O is organised into 5 groups of 8 bits. Each I/O channel may be configured as an input or an output. The board also includes the facility to define the power-up/reset state of a group of output bits. This is extremely useful in ensuring the safe start-up of a PC-controlled system. The 3 counter/timers are implemented using the industry-standard 8254 device. One timer can be used as a periodic interrupt generator while the other two timers can be connected to external signals for frequency measurement and pulse generation.

The D-50 I/O connector conforms to Arcom's standard Signal Conditioning System (SCS) and may be used to drive a range of Signal Conditioning Boards (SCB); see Arcom's PCbus catalogue for more details.

Features

- CE compliant design
- 40-channel digital I/O
- Three 16-bit counter/timers with max count rate (input and output) 1MHz
- Compact I/O addressing scheme (link selectable base address)
- Link-selectable interrupt options (IRQ2,3,4,5,7)
- Each channel has a current sink capability of 24mA @ 0.45V
  and source current of 500µA @ 2.7V
- Bit programmable for input or output
- Group selection of powerup/reset state.
- Board access LED (for all decoded addresses)
- User controlled LED
- 8-bit bus interface
- I/O connector conforms to Arcom Signal Conditioning System (SCS)
- Operating temperature range, +5°C to +55°C
- Power consumption from the host, max 300mA @ +5V
- MTBF: 477,000 hours (using generic figures from MIL-HDBK-217F at ground benign)

Getting Started

- Switch off PC
- Install Board in supplied configuration
- Switch on PC
- Run TEST.EXE (supplied on utility disk)
- An access/user LED should flash. If not check default link configuration. (Page 7)

Microsoft WindowsNT

FREE Windows NT4.0 Drivers

Visit the 'PC(ISA)bus Boards' page on the Arcom Website, www.arcom.co.uk/ntdrv10_AR.exe to download.

Operation

Reading or Writing to the Board

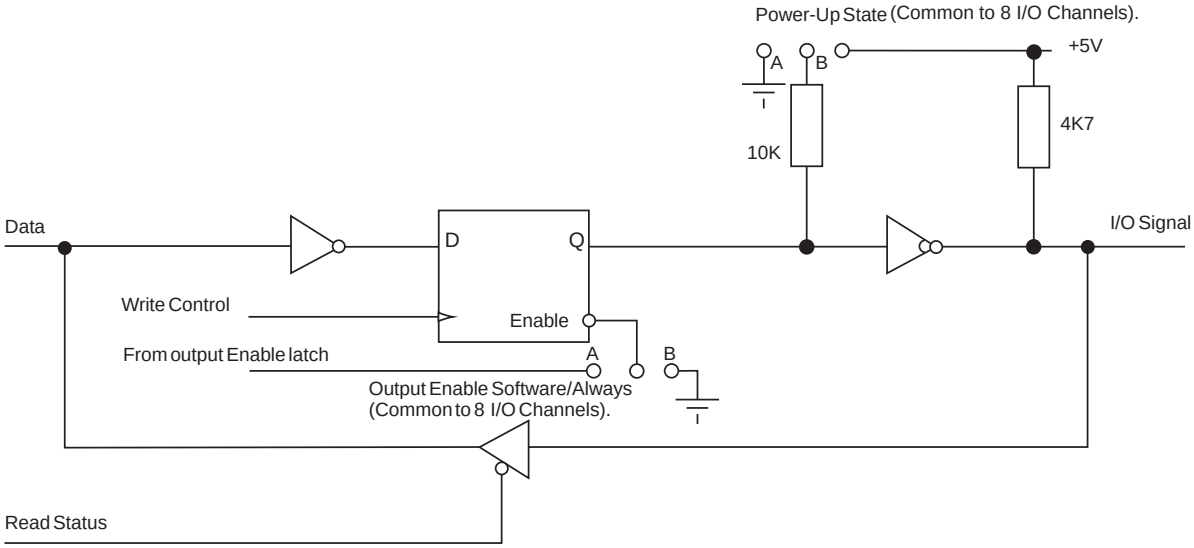
Control of the PCIB40 is achieved by writing to a **pointer register** and then accessing a **data register** to read or write the required I/O register. The pointer register need only be written with a new value if a different register is to be accessed. The board occupies only two bytes of PCbus I/O space. Each time the board is accessed, the red LED will flash momentarily.

Digital I/O channels

To use a digital channel (or bit) as an output simply write to that channel (or bit). To use a digital channel (or bit) as an input write a ‘1’ to the channel to initialise . Thereafter a read can be used. You can configure each digital channel (or bit) as an input or an output but it is advisable to configure the board in groups. e.g. Group 1,2 & 3 output, Group 4 & 5 input. When an output is set to ‘0’ (logic low) it is not advisable to attempt to drive the external connection to logic high.

Reading a digital channel, when it is an output, will return the state of the output. This can be useful if you need to check the status of an output.

Electrical configuration of each digital channel:



Power-up or reset state of outputs

When digital I/O boards are used to control large or crucial items of plant, it is often necessary to define how the output lines power-up. This is because it can take many seconds to boot an operating System and run an application program from reset and begin initialising the system. Each **group of eight** I/O signals can be selected to be a logical ‘0’, a logical ‘1’ or ‘don’t care’ at power-up or on reset. This is configured using jumpers (see links section).

To use this feature set the links for the power-up or reset condition required. Then in your code write to the group registers the output levels required, and finally enable the outputs by writing a ‘1’ to bit 0 of register 90 (hex).

Note: This feature is suited to outputs not inputs. Setting an input to a power-up state of ‘0’ will require the group register being written with all ‘1’s’ to enable the use of the channels as inputs.

Counter Timers

The PCIB40 includes three programmable 16-bit counter/timers. Counter 0 may be driven by either a 10KHz, 100KHz or 1MHz clock and can be used to generate regular interrupts. An interrupt is generated **only** when the counter 0 output goes to a '1'.

The input and gate control signals of counters 1 and 2 are connected as inputs from the D-50 while the counter outputs are linkable to the D-50 connector. Counter inputs 1 and 2 may be used for frequency or pulse measurement and the outputs used for pulse generation. Refer to the link section and pin assignments table for connection details.

I/O map

The value written to the pointer register is used to select the on-board I/O location to be accessed. This board occupies two consecutive addresses and has nine I/O function registers and three special function registers.

The board must be set on an **even** address boundary. (i.e. 180h, 182h, 200h etc.)

Address	Read/write	Register Name	Register Function
Base (180h)	Write Only	Pointer Register	On-board register (e.g. 80h)
Base+1 (181H)	Read/Write	Data Register	Data to Read/Write from/to register

I/O Function Registers

Pointer Value (hex)	Read/Write	Pointer Name	Pointer Bit	Functions
00	Write	Output Control Latches Group 0	Bit 0-7	0= Output '0' 1= Output '1'
00	Read	Status of Group 0	Bit 0-7	0= Input '0' 1= Input '1'
01	Write	Output Control Latches Group 1	Bit 0-7	0= Output '0' 1= Output '1'
01	Read	Status of Group 1	Bit 0-7	0= Input '0' 1= Input '1'
02	Write	Output Control Latches Group 2	Bit 0-7	0= Output '0' 1= Output '1'
02	Read	Status of Group 2	Bit 0-7	0= Input '0' 1= Input '1'
03	Write	Output Control Latches Group 3	Bit 0-7	0= Output '0' 1= Output '1'
03	Read	Status of Group 3	Bit 0-7	0= Input '0' 1= Input '1'
04	Write	Output Control Latches Group 4	Bit 0-7	0= Output '0' 1= Output '1'
04	Read	Status of Group 4	Bit 0-7	0= Input '0' 1= Input '1'
05 - 0F		Not Used		
10	Read/Write	Counter/timer 0 Access	Bit 0-7	See data sheet 8254*
11	Read/Write	Counter/timer 1 Access	Bit 0-7	See data sheet 8254*
12	Read/Write	Counter/timer 2 Access	Bit 0-7	See data sheet 8254*
13	Write	Counter/Timer Control Word	Bit 0-7	See data sheet 8254*

* A copy of the 8254 (71054) data sheet may be obtained from our Customer Support team (Tel: 01223 412 428)

Special Function Registers

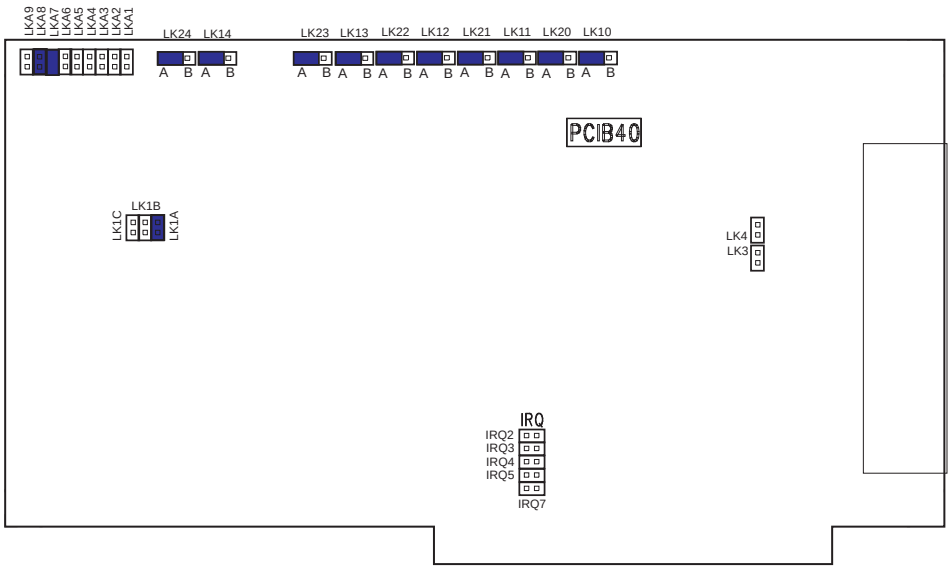
The green User LED is controlled by bit 0 when the pointer register is loaded with 80h.The board identification register can be used to confirm that the board is present in the system and is the correct board type. Other PCbus I/O boards in Arcom's range will return a different value.

Pointer Value (hex)	Read/Write	Pointer Name	Pointer Bit	Functions
80	Write	User LED Control	Bit 0 Only	1=LED ON 0=LED OFF
81	Read	Board Identification	Bit 0-7	Always 00 for the PCIB40
90	Write	Output Enable Control	Bit 0 Only	0=Disabled 1=Enabled

Links

Throughout this section a '+' indicates a default link.

Default Link Position Diagram



Base Address Select

Links LKA1-9

The base address of the PCIB40 is set using the link area shown below:

Note: When a link is fitted the address line is decoded as a '1' and when the link is omitted the address line is decoded as a '0'.

The default address is set to 180h

Link	Address Line
LKA9	A9
+ LKA8	A8
+ LKA7	A7
LKA6	A6
LKA5	A5
LKA4	A4
LKA3	A3
LKA2	A2
LKA1	A1

Link 1 Counter 0 Clock Frequency Select

The clock input for counter 0 can be connected to an on-board clock generator operating at either 10KHz, 100KHz or 1MHz. This is set using LK1A/B/C.

+	LK1A	Clock input = 1MHz
	LK1B	Clock input = 100KHz
	LK1C	Clock input = 10KHz

Links 10-14 Power-Up Output State

These links are used to select the power-up state of the five groups of I/O channels. For more information see page 4.

+	LK10	*Position A* for Group 0 outputs set to ‘1’ *Position B* for Group 0 outputs reset to ‘0’
+	LK11	*Position A* for Group 1 outputs set to ‘1’ *Position B* for Group 1 outputs reset to ‘0’
+	LK12	*Position A* for Group 2 outputs set to ‘1’ *Position B* for Group 2 outputs reset to ‘0’
+	LK13	*Position A* for Group 3 outputs set to ‘1’ *Position B* for Group 3 outputs reset to ‘0’
+	LK14	*Position A* for Group outputs 4 set to ‘1’ *Position B* for Group outputs 4 reset to ‘0’

Links 20-24 Power-up control

Select whether the output buffer is always enabled or controlled by software. If you are configuring the board for known boot up state then the group must be software enabled. If link B is fitted the output state cannot be determined (‘don’t care’ state) at power up or reset.

+	LK20	*Position A* Group 0 Outputs enabled by ‘software’ *Position B* Group 0 Outputs always enabled after power on/reset
+	LK21	*Position A* Group 1 Outputs enabled by ‘software’ *Position B* Group 1 Outputs always enabled after power on/reset
+	LK22	*Position A* Group 2 Outputs enabled by ‘software’ *Position B* Group 2 Outputs always enabled after power on/reset
+	LK23	*Position A* Group 3 Outputs enabled by ‘software’ *Position B* Group 3 Outputs always enabled after power on/reset
+	LK24	*Position A* Group 4 Outputs enabled by ‘software’ *Position B* Group 4 Outputs always enabled after power on/reset

Link IRQ2-5 & 7 Interrupt select

The output of counter 0 can be used to generate an interrupt on either IRQ 2,3,4,5 or 7.

NOTE: A PC must be configured with only one interrupt source for each interrupt line. Check your PC configuration before selecting the interrupt signal. If you are not using the interrupt facility, it is recommended that the jumper is not fitted.

IRQ2	Timer interrupt on IRQ2
IRQ3	Timer interrupt on IRQ3
IRQ4	Timer interrupt on IRQ4
IRQ5	Timer interrupt on IRQ5
IRQ7	Timer interrupt on IRQ7

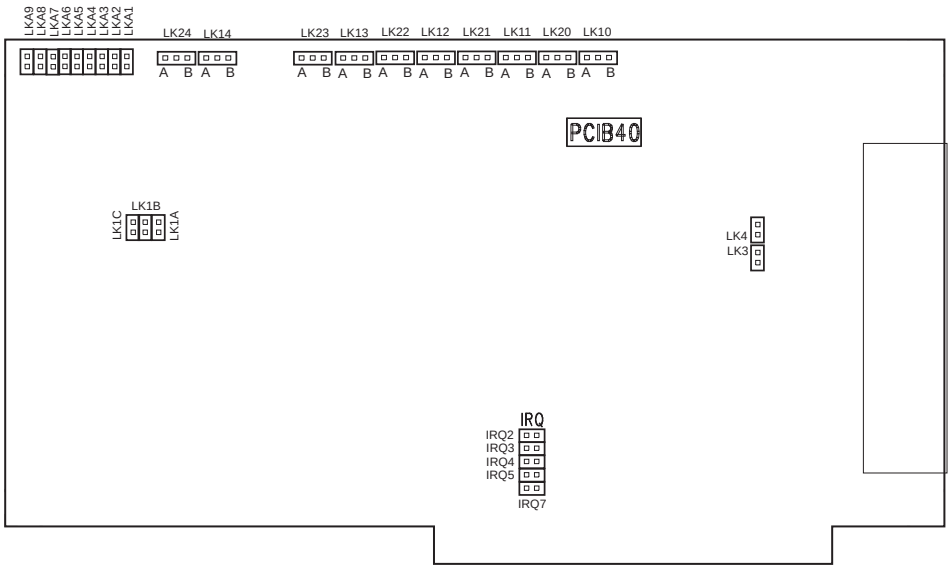
Links 3 & 4 Counter 1 and 2 Output Select

The outputs from counter 1 and 2 can be connected to the D-50 connector using LK4 and 3 respectively.

NOTE: The counter outputs are interfaced to the I/O connector using an inverting open-collector driver. The output state is therefore the inverse of the counter output state defined in the data sheet. When using the counter outputs, it is necessary to ensure that the I/O signals for group 2, bits 0 and 1, are set for input mode by writing '1's to both bits. This avoids the counter output conflicting with the I/O port output.

LK3	Connects T2 output via inverter buffer, to RC24 (Digital group 2, bit 1)
LK4	Connects T1 output via inverter buffer, to RC23 (Digital group 2, bit 0)

User Configuration Record Diagram



Link	Default	User
LKA1		
LKA2		
LKA3		
LKA4		
LKA5		
LKA6		
LKA7		
LKA8		
LKA9		
LK10		
LK11		
LK12		
LK13		
LK14		
LK20		

Link	Default	User
LK21		
LK22		
LK23		
LK24		
LK1A		
LK1B		
LK1C		
LK3		
LK4		
IRQ2		
IRQ3		
IRQ4		
IRQ5		
IRQ3		
IRQ7		

D-50 Output Connector (PL2) Pin Assignments

The pin assignments are listed with the pin number of the D-50 connector and also the pin number when a 50-way IDC ribbon cable is connected to the D-50. The pin assignments conform to the Arcom Signal Conditioning System (SCS) and may be connected to an external Signal Conditioning Board.

Ribbon Cable No.	D-50 Pin No.	Function	Alternative Function
1	1	0V	
2	34	0V	
3	18	Group 0 - Bit 0	
4	2	Group 0 - Bit 1	
5	35	Group 0 - Bit 2	
6	19	Group 0 - Bit 3	
7	3	Group 0 - Bit 4	
8	36	Group 0 - Bit 5	
9	20	Group 0 - Bit 6	
10	4	Group 0 - Bit 7	
11	37	0V	
12	21	Group 4 - Bit 0	
13	5	Group 1 - Bit 0	
14	38	Group 1 - Bit 1	
15	22	Group 1 - Bit 2	
16	6	Group 1 - Bit 3	
17	39	Group 1 - Bit 4	
18	23	Group 1 - Bit 5	
19	7	Group 1 - Bit 6	
20	40	Group 1 - Bit 7	
21	24	0V	
22	8	Group 4 - Bit 1	
23	41	Group 2 - Bit 0	Counter 1 Output (LK4)
24	25	Group 2 - Bit 1	Counter 2 Output (LK3)
25	9	Group 2 - Bit 2	
26	42	Group 2 - Bit 3	
27	26	Group 2 - Bit 4	
28	10	Group 2 - Bit 5	
29	43	Group 2 - Bit 6	
30	27	Group 2 - Bit 7	
31	11	0V	
32	44	Group 4 - Bit 2	
33	28	Group 3 - Bit 0	Counter 1 Gate Input
34	12	Group 3 - Bit 1	Counter 1 Clock Input
35	45	Group 3 - Bit 2	Counter 2 Gate Input
36	29	Group 3 - Bit 3	Counter 2 Clock Input
37	13	Group 3 - Bit 4	
38	46	Group 3 - Bit 5	
39	30	Group 3 - Bit 6	
40	14	Group 3 - Bit 7	
41	47	0V	
42	31	Group 4 - Bit 3	
43	15	Group 4 - Bit 4	
44	48	Group 4 - Bit 5	
45	32	Group 4 - Bit 6	
46	16	Group 4 - Bit 7	
47	49	-12V	
48	33	+12V	
49	17	+5V	
50	50	+5V	

Installation for CE Compliance

To maintain compliance with the requirements of the EMC Directive (89/336/EEC), this product must be correctly installed. The PC in which the board is housed must be CE compliant as declared by the PC manufacturer. The type of external I/O cable can be chosen according to the notes below:

1. Remove the cover of the PC observing any additional instructions of the PC manufacturer
2. Locate the board in a spare ISA slot and press gently but firmly into place
3. Ensure that the metal bracket attached to the board is fully seated
4. Fit the bracket clamping screw and firmly tighten this on the bracket

   NOTE: Good contact of the bracket to chassis is essential
5. Replace the cover of the PC observing any additional instructions of the PC manufacturer

Cable

Cable length 1Metre or less	:	Ribbon cable satisfactory
Cable length 1M to 3M	:	Commercial screened cable gives the protection required
Longer cable or noisy environment	:	Use fully screened cable with metal backshells e.g. Arcom CAB50CE

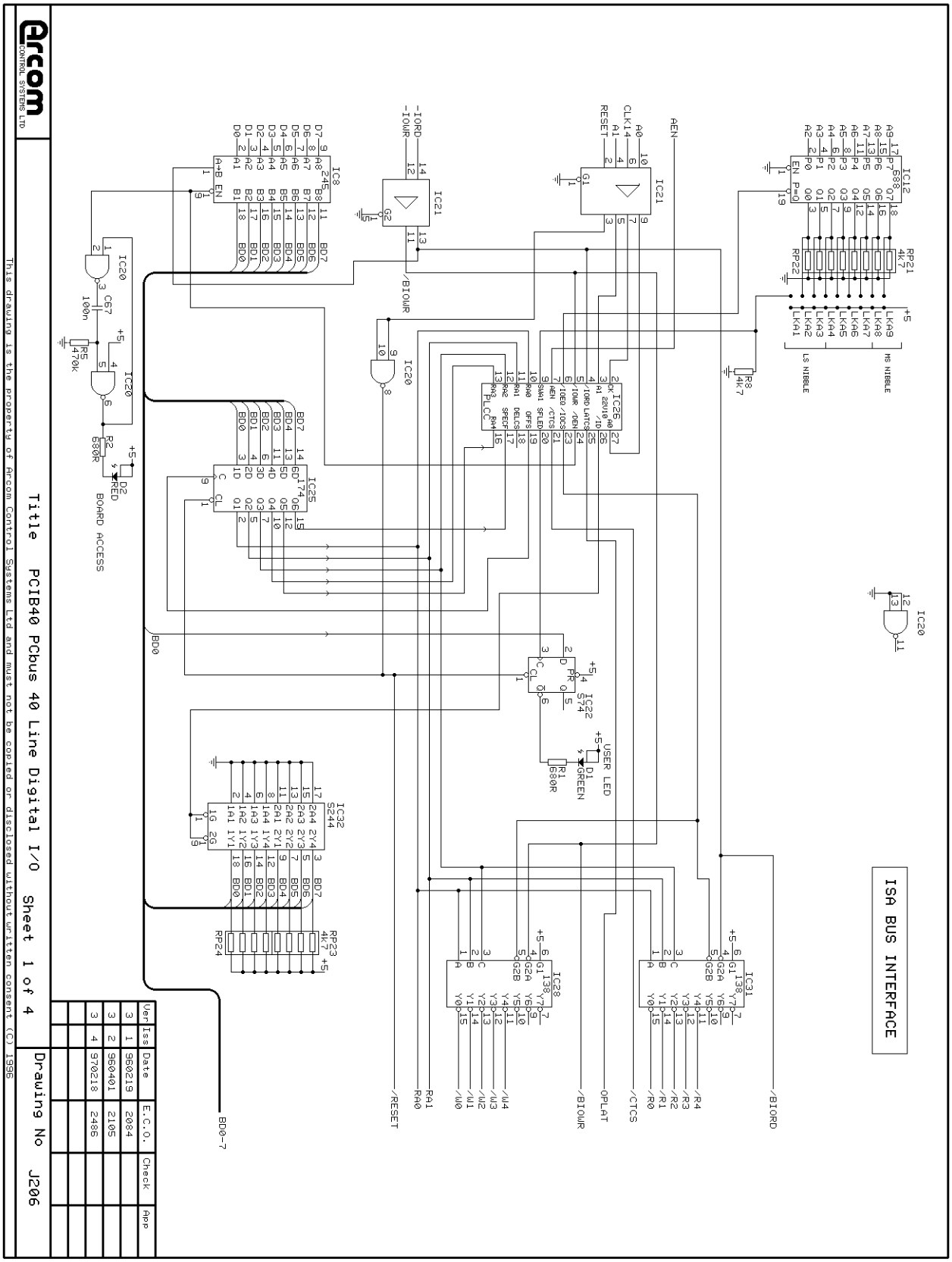
The following standards have been applied to this product:

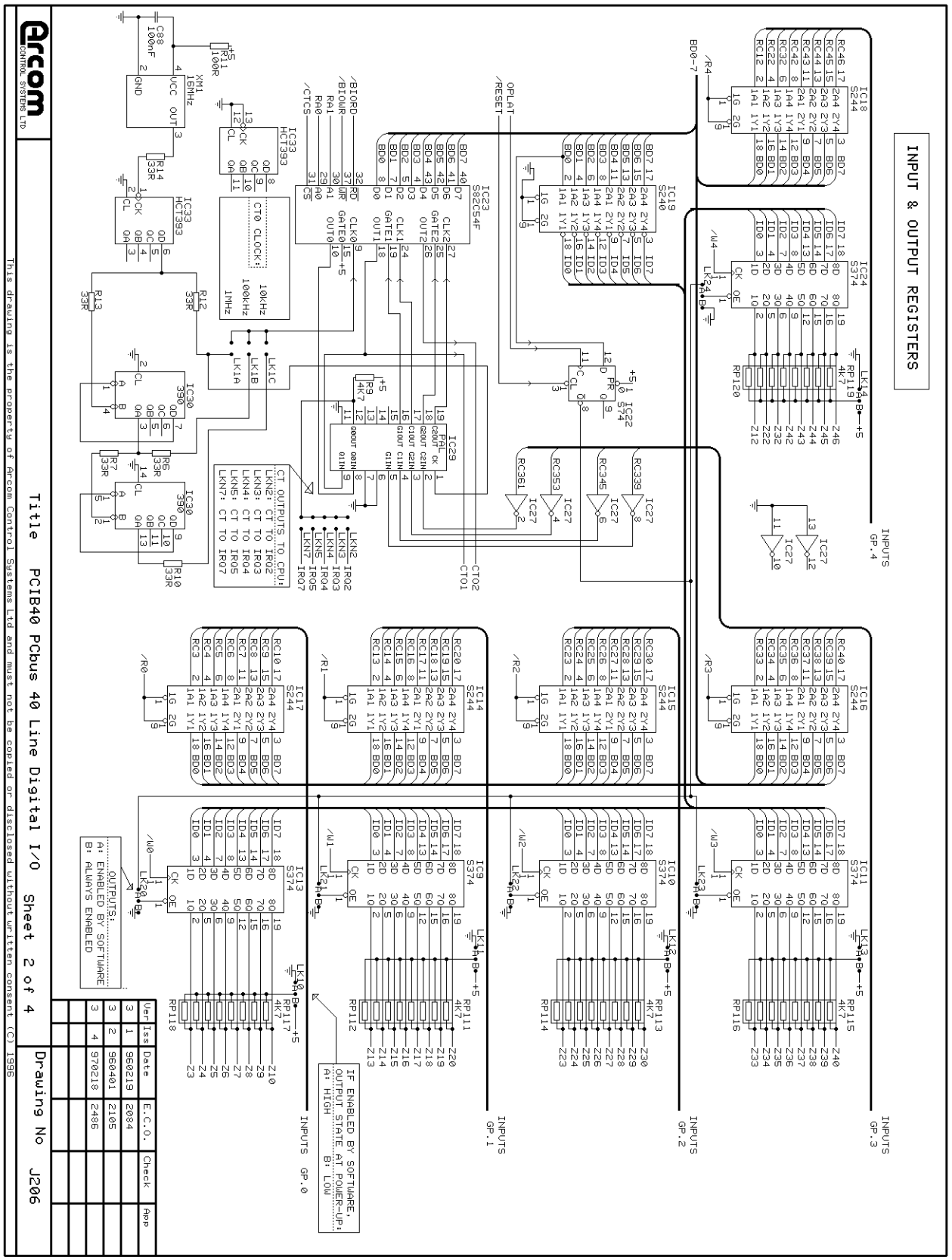
BS EN50081-1: 1992 Generic Emissions Standard, Residential, Commercial, Light Industry

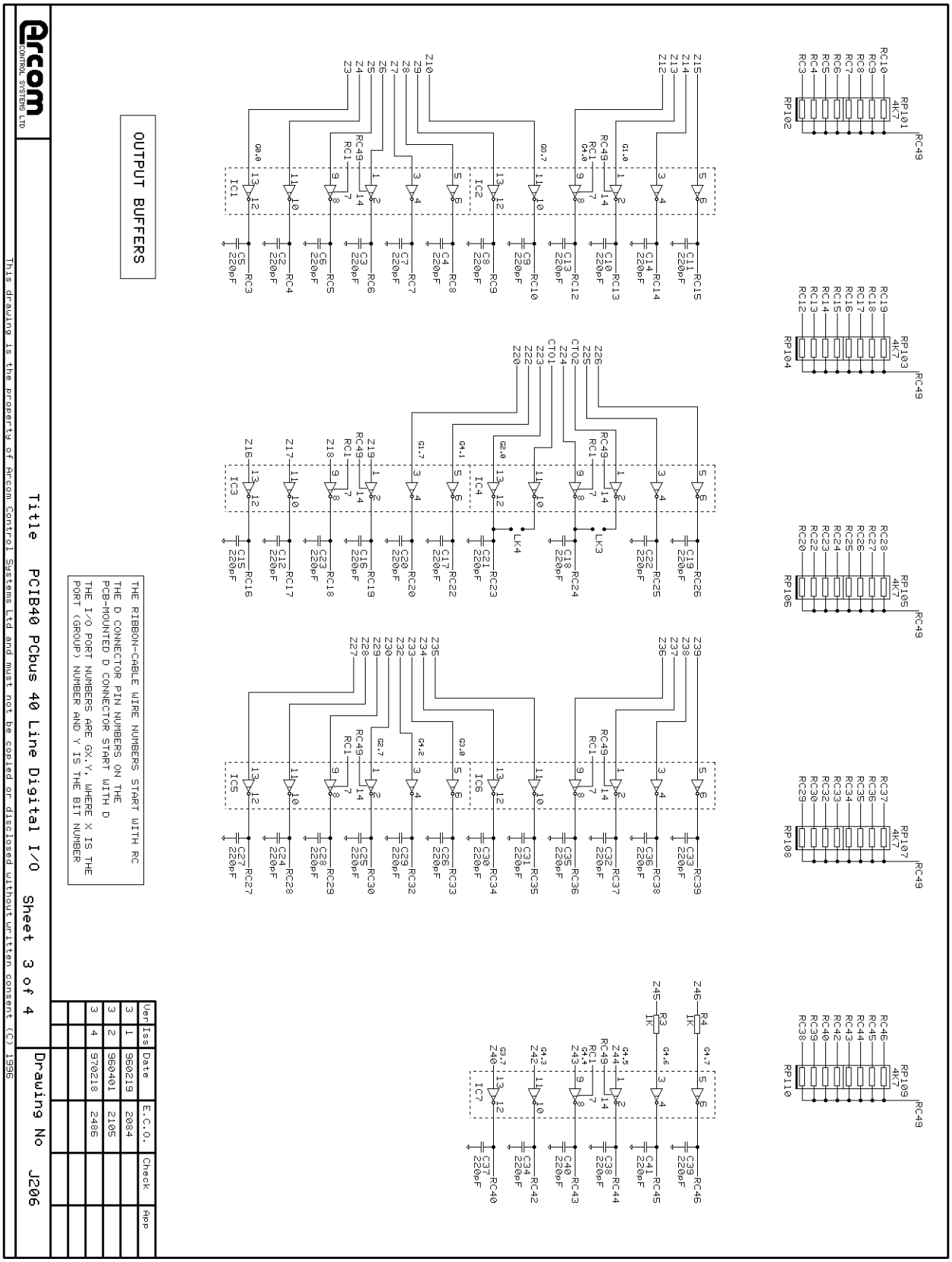
BS EN50082-1: 1992 Generic Immunity Standard, Residential, Commercial, Light Industry

BS EN55022 : 1995 ITE Emissions, Class B, Limits and Methods

Circuit Diagrams




INPUT & OUTPUT REGISTERS
Title PCIB40 PCbus 40 Line Digital I/O Sheet 2 of 4
Drawing No J206
This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent (C) 1995
INPUTS GP.4
INPUTS GP.3
INPUTS GP.2
INPUTS GP.1
INPUTS GP.0
OUTPUTS:
A: ENABLED BY SOFTWARE
B: ALWAYS ENABLED
IF ENABLED BY SOFTWARE:
OUTPUT STATE AT POWER-UP:
A: HIGH
B: LOW
CT OUTPUTS TO CPU:
LKN2: CT TO IR02
LKN3: CT TO IR03
LKN4: CT TO IR04
LKN5: CT TO IR05
LKN7: CT TO IR07
CT0 CLOCK: 10kHz 100kHz 1MHz
Ver Iss Date E.C.O. Check App
3 1 960219 2084
3 2 960401 2105
3 4 970218 2486


OUTPUT BUFFERS
THE RIBBON-CABLE WIRE NUMBERS START WITH RC
THE D CONNECTOR PIN NUMBERS ON THE PCB-MOUNTED D CONNECTOR START WITH D
THE I/O PORT NUMBERS ARE GX.Y, WHERE X IS THE PORT (GROUP) NUMBER AND Y IS THE BIT NUMBER
Arcom CONTROL SYSTEMS LTD.
Title PCIB40 PCbus 40 Line Digital I/O Sheet 3 of 4
Drawing No J206
Ver Iss Date E.C.O. Check App
3 1 960219 2084
3 2 960401 2105
3 4 970218 2486
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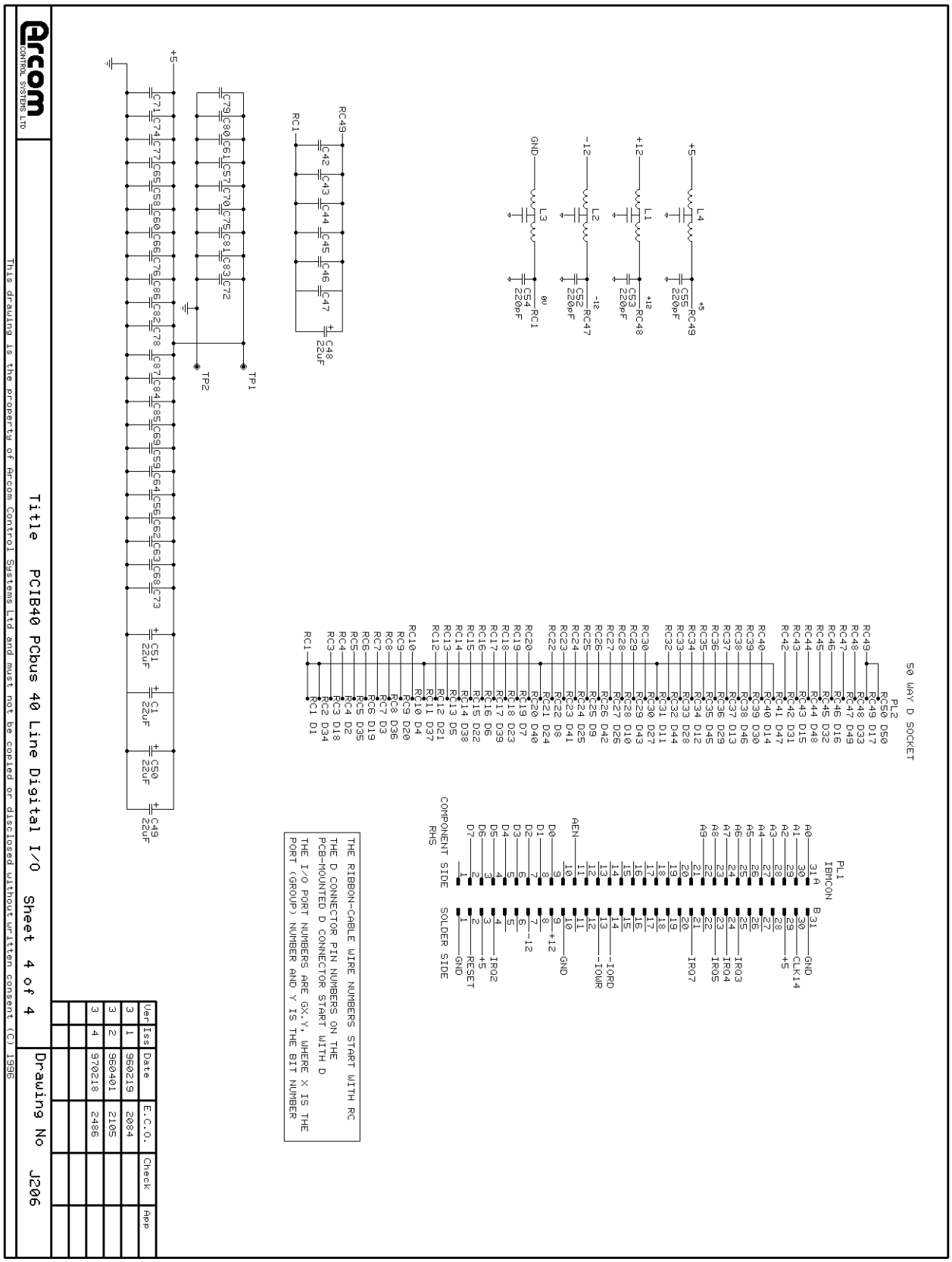
50 WAY D SOCKET
PL2
IBMCON
PL1
THE RIBBON-CABLE WIRE NUMBERS START WITH RC
THE D CONNECTOR PIN NUMBERS ON THE
PCB-MOUNTED D CONNECTOR START WITH D
THE I/O PORT NUMBERS ARE GX.Y, WHERE X IS THE
PORT (GROUP) NUMBER AND Y IS THE BIT NUMBER
COMPONENT SIDE
SOLDER SIDE
Arcom CONTROL SYSTEMS LTD
Title PCIB40 PCbus 40 Line Digital I/O Sheet 4 of 4
Drawing No J206
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3	2	950401	2105		
3	4	970218	2486		

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